IN THE CLAIMS:

Please amend claims 1 and 13, as set forth below.

1. (Currently Amended) A method comprising:

depositing a layer of a metal on each of a number of conductors disposed on a surface of a first wafer;

aligning the first wafer with a second wafer, the second wafer having a number of conductors disposed on a surface thereof;

directly contacting the metal layer on each of the conductors of the first wafer with a mating one of the conductors on the second wafer; and

forming a bond between the metal layer on each of the conductors of the first wafer and the mating one conductor of the second wafer.

2. (Previously Presented) The method of claim 1, further comprising, prior to depositing the metal layer on each of the conductors of the first wafer, removing dielectric material from the surface of the first wafer.

3. (Previously Presented) The method of claim 1, further comprising, prior to depositing the metal layer on each of the conductors of the first wafer, removing native oxide from the conductors.

4. (Previously Presented) The method of claim 1, wherein the conductors of the first wafer comprise Copper.

5. (Previously Presented) The method of claim 1, wherein the metal comprises a metal selected from a group consisting of Silver, Gold, Ruthenium, Osmium, Iridium, Palladium, Rhodium, and Platinum.

6. (Previously Presented) The method of claim 1, wherein the bond is formed at a temperature between approximately 100 and 300 degrees Celsius.

7. (Previously Presented) The method of claim 1, wherein depositing the layer of metal on each of the conductors of the first wafer comprises:
forming a blanket layer of the metal over the conductors and the surface of the first wafer; and
removing the metal from at least portions of the first wafer surface.

8. (Previously Presented) The method of claim 1, wherein depositing the layer of metal on each of the conductors of the first wafer comprises selectively depositing the metal on each of the conductors.

9. (Previously Presented) The method of claim 8, wherein selectively depositing the metal on each of the conductors of the first wafer comprises an electroless plating process, an electroplating process, or a contact displacement plating process.

10. (Previously Presented) The method of claim 1, wherein the metal layer on each of the conductors of the first wafer comprises a number of islands.

11. (Previously Presented) The method of claim 10, wherein the islands are selectively deposited on each of the conductors of the first wafer.

12. (Previously Presented) The method of claim 10, wherein the islands are formed by a process comprising:

depositing a blanket layer of the metal over the conductors and the surface of the first wafer; and

removing the blanket metal layer from at least portions of the first wafer surface and from portions of each conductor to form the number of islands on each conductor.

13. (Currently Amended) A method comprising:
depositing a layer of a first metal on each of a number of conductors disposed on a first wafer;
depositing a layer of a second metal on each of a number of conductors disposed on a second wafer;
aligning the first wafer with the second wafer;
directly contacting the metal layer on each of the conductors of the first wafer with the metal layer on a mating one of the conductors of the second wafer; and
forming a bond between the metal layer on each of the conductors of the first wafer and the metal layer on the mating one conductor of the second wafer.

14. (Previously Presented) The method of claim 13, further comprising, prior to depositing the metal layer on each of the conductors of at least one of the first and second wafers, removing dielectric material from a surface of the at least one wafer.

15. (Previously Presented) The method of claim 13, further comprising, prior to depositing the metal layer on each of the conductors of at least one of the first and second wafers, removing native oxide from the conductors of the at least one wafer.

16. (Original) The method of claim 13, wherein the conductors of each of the first and second wafers comprise the same metal.

17. (Original) The method of claim 16, wherein the conductors of each of the first and second wafers comprise Copper.

18. (Original) The method of claim 13, wherein the first metal and the second metal are the same.

19. (Original) The method of claim 13, wherein the first metal and the second metal are different.

20. (Previously Presented) The method of claim 13, wherein each of the first and second metals comprises a metal selected from a group consisting of Silver, Gold, Ruthenium, Osmium, Iridium, Palladium, Rhodium, and Platinum.

21. (Previously Presented) The method of claim 13, wherein the bond is formed at a temperature between approximately 100 and 300 degrees Celsius.

22. (Previously Presented) The method of claim 13, wherein depositing the metal layer on each of the conductors of at least one of the first and second wafers comprises:

forming a blanket metal layer over the conductors and a surface of the wafer; and

removing the blanket metal layer from at least portions of the wafer surface.

23. (Previously Presented) The method of claim 13, wherein depositing the metal layer on each of the conductors of at least one of the first and second wafers comprises selectively depositing the metal layer on the conductors.

24. (Previously Presented) The method of claim 23, wherein selectively depositing the metal layer on each of the conductors comprises an electroless plating process, an electroplating process, or a contact displacement plating process.

25. (Previously Presented) The method of claim 13, wherein the metal layer on each of the conductors of at least one of the first and second wafers comprises a number of islands.

26. (Original) The method of claim 25, wherein the islands are selectively deposited on the conductors.

27. (Previously Presented) The method of claim 25, wherein the islands are formed by a process comprising:

depositing a blanket metal layer over each of the conductors and a surface of the wafer; and

removing the blanket metal layer from at least portions of the wafer surface and from portions of each conductor to form the number of islands on each conductor.

28. (Withdrawn) A wafer stack comprising:

a first wafer including a number of conductors disposed on a surface of the first wafer, each of the conductors having a layer of metal formed thereon; and

a second wafer including a number of conductors disposed on a surface of the second wafer, each of the conductors having a layer of metal formed thereon;

wherein the metal layer of each conductor of the first wafer is bonded to the metal layer on a corresponding conductor of the second wafer.

29. (Withdrawn) The wafer stack of claim 28, wherein the conductors on each of the first and second wafers comprise the same metal.

30. (Withdrawn) The wafer stack of claim 29, wherein the conductors on each of the first and second wafers comprise Copper.

31. (Withdrawn) The wafer stack of claim 28, wherein the metal layer on each conductor of the first wafer and the metal layer on each conductor of the second wafer comprises the same metal.

32. (Withdrawn) The wafer stack of claim 28, wherein the metal layer on each conductor of the first wafer comprises a first metal and the metal layer on each conductor of the second wafer comprises a second, different metal.

33. (Withdrawn) The wafer stack of claim 28, wherein the metal layer on each conductor on each of the first and second wafers comprises one of Silver, Gold, Ruthenium, Osmium, Iridium, Palladium, Rhodium, and Platinum.

34. (Withdrawn) The wafer stack of claim 28, wherein the first and second wafers comprise the same material.

35. (Withdrawn) The wafer stack of claim 28, wherein the first wafer comprises one material and the second wafer comprises a different material.

36. (Withdrawn) The wafer stack of claim 28, wherein the first wafer includes logic circuitry and the second wafer includes memory circuitry.

37. (Withdrawn) A wafer stack comprising:

a first wafer, the first wafer having an interconnect including an uppermost dielectric layer and a number of lower dielectric layers, each lower dielectric layer including a number of conductors comprised of a first metal and the uppermost dielectric layer including a number of conductors comprised of a third metal; and

a second wafer, the second wafer having an interconnect including an uppermost dielectric layer and a number of lower dielectric layers, each lower dielectric layer including a number of conductors comprised of a second metal and the uppermost dielectric layer including a number of conductors comprised of a fourth metal;

wherein the conductors comprised of the third metal and the conductors comprised of the fourth metal are capable of bonding together at a temperature of approximately 300° Celsius or less; and

wherein the conductors of the uppermost dielectric layer of the first wafer are bonded to the conductors of the uppermost dielectric layer of the second wafer.

38. (Withdrawn) The wafer stack of claim 37, wherein the first and second metals comprise the same metal.

39. (Withdrawn) The wafer stack of claim 38, wherein the first and second metals comprise Copper.

40. (Withdrawn) The wafer stack of claim 37, wherein the third and fourth metals comprise the same metal.

41. (Withdrawn) The wafer stack of claim 37, wherein each of the third and fourth metals comprise one of Silver, Gold, Ruthenium, Osmium, Iridium, Palladium, Rhodium, Platinum.

42. (Withdrawn) The wafer stack of claim 37, wherein the third metal comprises one of Silver, Gold, Ruthenium, Osmium, Iridium, Palladium, Rhodium, Platinum and the fourth metal comprises Copper.